What is claimed is:

1. A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter.

2. A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises:

an inverter chain containing not less than one inverter; and

a metal-oxide-semiconductor capacitor, known as a MOS capacitor, connected to an output section of the inverter and exhibiting changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage.

3. A delay circuit according to claim 1, wherein a ratio of a gate voltage range of

an on-state MOS capacitor to a gate voltage range of an off-state MOS capacitor is proportional to an increment or a decrement of the source voltage during a transition period of a signal that appears in the output section of the inverter.

4. A delay circuit according to claim 1, wherein a value of the MOS capacitor changes in a direction to increase its capacitance during a transition period of a signal that appears in the output section of the inverter.

5. A delay circuit according to claim 1, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose gate is connected to a node that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential.

6. A delay circuit according to claim 1, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose gate is connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a ground potential.

7. A delay circuit according to claim 1, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source voltage.

8. A delay circuit according to claim 1, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of a logic signal from a high level to a low level, and whose gate is fixed at a ground potential.

9. A delay circuit according to claim 2, wherein a ratio of a gate voltage range of an on-state MOS capacitor to a gate voltage range of an off-state MOS capacitor is proportional to an increment or a decrement of the source voltage during a transition period of a signal that appears in the output section of the inverter.

10. A delay circuit according to claim 2, wherein a value of the MOS capacitor

changes in a direction to increase its capacitance during a transition period of a signal that appears in the output section of the inverter.

11. A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose gate is connected to a node that changes a logic level of the logic signal from a low level to a high level, and whose source and whose drain are fixed at a ground potential.

12. A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose gate is connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose source and drain are fixed at a ground potential.

13. A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by an n-MOS transistor whose source and drain are connected to a node that changes a logic level of the logic signal from a high level to a low level, and whose gate is fixed at a source

voltage.

14. A delay circuit according to claim 2, wherein the MOS capacitor is a node disposed on a transmission path of a logic signal, and is represented by a p-MOS transistor whose source and drain are connected to a node that changes a logic level of a logic signal from a high level to a low level, and whose gate is fixed at a ground potential.

15. A delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises:

an inverter chain containing not less than one inverter; and

a p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, to comprise the inverter, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions.

16. A method for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising the steps of:

(a) setting a metal-oxide-semiconductor capacitor disposed on a transmission

path of a logic signal to an off-state in an initial stage; and

(b) changing the metal-oxide-semiconductor capacitor to an on-state from the off-state according to a logic level of the logic signal.

17. A method according to claim 16, wherein the metal-oxide-semiconductor capacitor changes its capacitance in a direction of increasing values, during a transition period of a signal that appears on a node connected to the metal-oxide-semiconductor capacitor and disposed on a transmission path of a logic signal.